

1

HIGH-SPEED HIGH-POWER SEMICONDUCTOR DEVICES

CLAIM OF PRIORITY UNDER 35 U.S.C. §119

The present Application for Patent claims priority to Provisional U.S. Application Ser. No. 61/444,072, entitled "HIGH-SPEED HIGH-POWER SEMICONDUCTOR DEVICES," filed Feb. 17, 2011, assigned to the assignee hereof, and expressly incorporated herein by reference.

BACKGROUND

I. Field

The present disclosure relates generally to electronics, and more specifically to semiconductor devices.

II. Background

Semiconductor devices such as transistors are commonly used in various active circuits such as power amplifiers. A power amplifier can provide amplification and high output power for a signal prior to transmission over the air. Hence, power amplifiers are used in virtually all wireless communication systems and in wireless devices as well as base stations.

A radio frequency (RF) power amplifier may impose conflicting requirements on transistors used to implement the power amplifier. For example, the high-speed RF power amplifier may require (i) a high breakdown voltage for the transistors in order to handle a large voltage swing and (ii) a high frequency of operation in order to handle an RF signal. For a transistor fabricated with a complementary metal oxide semiconductor (CMOS) integrated circuit (IC) process, the speed of the transistor may be increased by reducing the length of the gate. However, a shorter gate length also reduces the breakdown voltage of the transistor, which then limits the transistor's ability to handle a large voltage swing required for a power amplifier. Hence, it is difficult to obtain a high breakdown voltage and a high frequency of operation for CMOS transistors.

One conventional technique for achieving high speed and high output power for a power amplifier is to stack a number of transistors in a cascode configuration. Each transistor in the stack may then observe only a fraction of the output voltage swing. However, stacking transistors may result in degraded efficiency and a challenging circuit design in order to properly bias the transistors, avoid instability and oscillation, and simultaneously achieve high output power and efficiency. Another conventional technique for achieving high speed and high output power for a power amplifier is to construct transistors using a complicated device architecture. However, such a device architecture is often incompatible with standard CMOS process flow, which may require more mask and process steps to fabricate the transistors, may be difficult to integrate with conventional CMOS integrated circuits, and may result in higher cost. An RF power amplifier that is not difficult to fabricate and has low cost is thus highly desirable.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a schematic diagram of a power amplifier. FIG. 2 shows a conventional N-channel MOS (NMOS) transistor.

FIG. 3 shows a high-speed high-power NMOS transistor.

FIG. 4 shows a model of the high-speed high-power NMOS transistor in FIG. 3.

2

FIG. 5 shows a high-speed high-power NMOS transistor fabricated with a silicon-on-insulator (SOI) IC process.

FIG. 6 shows a top view of the NMOS transistor in FIG. 5.

FIGS. 7A, 7B and 7C show cross-sectional views of the NMOS transistor in FIG. 5 along different lines.

FIG. 8 shows a schematic diagram of a model of the NMOS transistor in FIG. 5.

FIGS. 9A and 9B show operation of the NMOS transistor in FIG. 5 in an ON state and an OFF state, respectively.

FIG. 10 shows a high-speed high-power NMOS transistor with two field gates.

FIG. 11 shows a high-speed high-power P-channel MOS (PMOS) transistor fabricated with a SOI IC process.

FIG. 12 shows a high-speed high-power NMOS transistor fabricated with a standard bulk CMOS process.

FIG. 13 shows a high-speed high-power PMOS transistor fabricated with a standard bulk CMOS process.

FIG. 14 shows a block diagram of a wireless communication device.

FIG. 15 shows a process for fabricating a high-speed high-power semiconductor device/MOS transistor.

DETAILED DESCRIPTION

The detailed description set forth below is intended as a description of exemplary designs of the present disclosure and is not intended to represent the only designs in which the present disclosure can be practiced. The term "exemplary" is used herein to mean "serving as an example, instance, or illustration." Any design described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other designs. The detailed description includes specific details for the purpose of providing a thorough understanding of the exemplary designs of the present disclosure. It will be apparent to those skilled in the art that the exemplary designs described herein may be practiced without these specific details. In some instances, well-known structures and devices are shown in block diagram form in order to avoid obscuring the novelty of the exemplary designs presented herein.

High-speed high-power semiconductor devices are described herein. These semiconductor devices may be operated as transistors. Hence, the terms "semiconductor device", "transistor", and "MOS transistor" are used interchangeably herein. The high-speed high-power semiconductor devices may be fabricated in standard CMOS processes and may have various desirable characteristics such as a high breakdown voltage and a high operating speed. These semiconductor devices may be suitable for use in high-speed RF power amplifiers, power management integrated circuits (PMICs), switches, codecs, and other active circuits requiring high speed and/or high output power.

FIG. 1 shows a schematic diagram of an exemplary design of a power amplifier 100 implemented with a single N-channel metal oxide semiconductor (NMOS) transistor 110. NMOS transistor 110 has its gate receiving an input RF signal (RFin), its source coupled to circuit ground, and its drain providing an output RF signal (RFout). An inductor 120 has one end coupled to a power supply (Vdd) and the other end coupled to the drain of NMOS transistor 110. The Vdd supply may be a battery supply or some other power supply.

Power amplifier 100 may also include other circuits not shown in FIG. 1. For example, power amplifier 100 may include an input impedance matching circuit having one end receiving the RFin signal and the other end coupled to the